ABSTRACT

A packaged semiconductor device (a wafer-level chip scale package) containing an adhesive film containing conductive particles sandwiched between a chip with Cu-based stud bumps and a substrate containing a bond pad. Some conductive particles are sandwiched between the stud bump and bond pad to create a conductive path. The wafer level chip scale package is manufactured without the steps of dispensing solder and reflowing the solder and can optionally eliminate the use of a redistribution trace. Using such a configuration increases the reliability of the wafer-level chip scale package